Sampled Analog driving of high framerate UHD displays

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Abstract

For current high-end displays, conventional data transports require parallel data-pairs plus equalization circuits to deliver the required video data to the edge of the display panel. These accommodations increase cost, power, and complexity.

HYPHY's revolutionary 'Sampled Analog' video transport is the solution to this impasse, demonstrably delivering 10X more video payload per "wire-Hertz" than conventional methods, meaning more image data can be transferred to the panel while decreasing the cost and power of display driving hardware.

Author Keywords

High Data Rate; Sampled Analog; Video Transport;

1. Introduction

Consumer demand for larger, higher resolution, higher frame rate, and higher color depth displays is driving the data-rates of the connected video systems to the limit of conventional solutions. At current high-end displays, conventional data transports require multiple parallel data-pairs plus equalization circuits per display driver to deliver the required video data. Introduction of increasingly complex AR / VR systems also dictate increasing framerate and resolution. These accommodations increase cost, power and complexity.

HYPHY's revolutionary 'Sampled analog' video transport (SAVT) is the solution to this impasse, so that more image data can be transferred to the panel while decreasing the cost and power consumption of display driving hardware.

In order to underline the analog transport benefits, HYPHY has developed a new, sampled analog, display driver IC (DDIC) and the associated video transmitter. An LCD panel (8K 120 Hz, 65" diagonal) has been equipped with an array of this new DDIC, and has subsequently been demonstrated in November 2024 to a select audience.

2. Market development

The past decade has shown unprecedented increase in video data-rates. Where in the early 1990s the TV resolution took its first steps beyond PAL / NTSC at 1080 interlaced lines (30 Hz) and 1920 pixels at 8 bits per pixel, data-rates were approximately 1.5 gigabits per second. From the early 2000s onward, the first 4K UHD TVs were shipped, raising the bit-rate to 15 Gbps. Demand for higher frame rates increases this to ~ 30 Gbps, while future 8K standards and high framerate, high resolution AR / VR systems and autostereoscopic displays push toward and beyond 100 Gbps. At increasing resolution, also the number of source drivers increases, mitigating the data-rate between timing controller (TCON) and display edge, but still required data-rates exceed the capability of P2P video transport, as shown in figure 1.

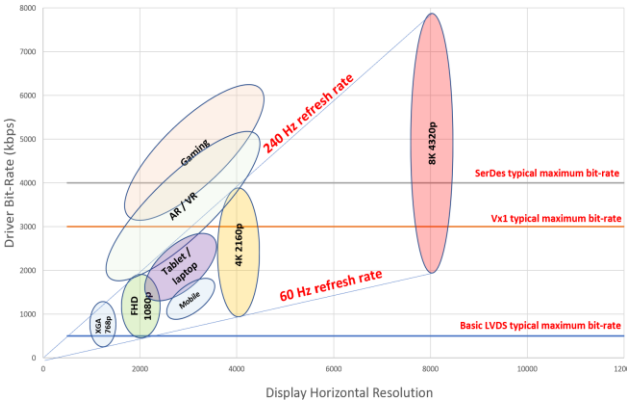

Figure 1: DDIC Bit rates for various resolution and frame-rates

3. Video Transport Principles

Within every display, digital sub-pixel values are distributed from the device input processor (SoC) to the edge of the display glass, where they must be converted into analog voltages that determine individual sub-pixel brightness.

Conventional video transports distribute the digital sub-pixel values to the edge of the display glass, converting to the analog domain at the last possible step in the process. The display industry's arsenal for accommodating exponentially growing video payloads (caused by increasing display resolution, refresh rates and bit-depth, driven by consumer expectation, but also by increasing demand for AR / VR displays, as indicated earlier) includes increasing clock rates, increasing the number of wire pairs, developing improved P2P communication protocols and possibly even applying video compression.

Response to the increased transfer speed so far has been to adopt this 'brute force' approach, that relies on high-speed digital semiconductors and protocols, with or without compression (simple LVDS→Vx1→proprietary P2P protocols) and multiple (up to 64) extreme-speed (>4 GHz) wire pairs to transport the sub-pixel values from SoC or graphics processor to the edge of the TFT panel through the display module's wiring harness (Fig. 2).

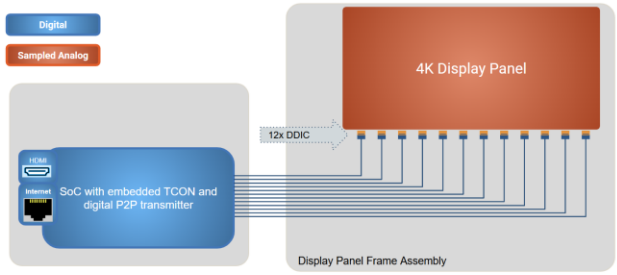

Figure 2: Brute Force Approach to 4K Digital Drive

Currently, several proprietary interfaces are in use, for example:

MIPI (Mobile Industry Processor Interface)

- Supports multiple display modes of operation including ultra-high definition video (8K and beyond), as well as power-efficient GUI and standby modes
- Highly power efficient in all modes of display operation
- Minimizes cost and complexity
- Highly scalable, supports all resolutions
- Incorporates VESA Display Stream Compression (DSC) and VESA Display Compression-M (VDC-M) standards

eDP (Embedded Display Port)

- High data transfer rate, supporting up to 8.64 Gbit/s with four data pairs.
- It is capable of transmitting video and audio signals, as well as data and control signals.
- eDP uses a low voltage differential signaling (LVDS) protocol, similar to LVDS, which allows for low power consumption and reduced electromagnetic interference.
- It supports high resolutions and frame rates, making it ideal for embedded systems and mobile devices that require high-quality display performance.
- eDP also has a feature called Multiple Independent Displays (MID), which allows for multiple displays to be driven from a single eDP interface, reducing the need for additional interfaces.

CEDS (Clock Embedded Differential Signal)

- Proprietary protocol developed by Lx Semicon. Promoted in Korea, LGD (KAIST)
- High speed (up to 2 Gbps) P2P interface
- Equalizer

USI-T (Unified Standard Interface for TV)

- Developed by Samsung
- High-speed 4Gbps intra-panel interface

CHPI (Proposed "China Point-to-Point Interface")

- Developed by BOE
- Packet based, no clock recovery
- Scalable up to 3.5 Gbps
- Low power
- Spread spectrum EMI reduction

CSPI (CSOT Point-to-Point Interface)

- Developed by TCL / CSOT
- Alternative proposed Standard Point to Point Interface for China
- Up to 48 Wire Pairs
- AEQ adaptive equalizer
- Up to 6 Gbps

The foregoing approaches increase cost and impose manufacturing complexity, such as equalization, rendering high frame-rate UHD televisions, monitors and AR/VR systems too expensive for mass market adoption. Developing compression algorithms may improve the headroom for throughput slightly but will certainly add to the cost and power consumption of video transport by integrating the decompression logic into each of the DDICs. Even with compression, data-rates are exceedingly high, with 4Gbps transmission on normal PCBAs being prone to unacceptable EMI emissions

The display industry is in urgent need of a much better video transport technology. HYPHY has developed a new approach which provides exactly that.

4. A Video Transport Innovation

The fundamental insight that drove HYPHY's breakthrough is that the requirements for bit-perfect, error-free machine-to-machine communication are fundamentally and dramatically different from the requirements for communicating video content to human eyes and human brains - to human cognitive systems. Machines require absolute precision. Human cognition is complex and resilient, while the TFT arrays are physical devices subject to intrinsic variability.

A single bit error in a sequence of symbols sent from one computer to another is usually unacceptable, because preservation of the payload is imperative. Human visual systems, however, are tolerant of video signal errors. Double-blind studies [1] have established that a given video signal can be measurably and objectively superior to another, yet the two can be completely indistinguishable to even discriminating viewers. Thus, imposing the unnecessary bit-perfection requirement on video transports imposes a costly and eventually unsustainable burden - a 'digital overhead' on video transports.

Based on this fundamental insight, HYPHY developed an error-tolerant 'sampled analog' video transport that allows 10× higher transmission rates (or 10× lower clock rates) than existing solutions along the same conductors [2] (Fig. 3).

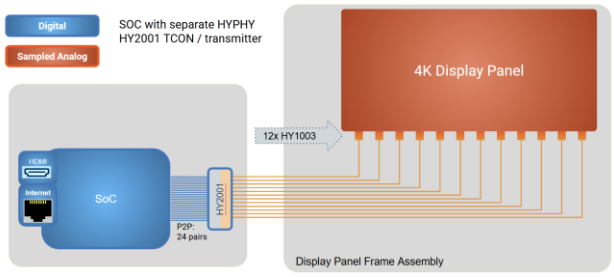

Figure 3: HYPHY SAVT Driving at Much Lower Signal Frequencies

Transporting video in the analog domain has an additional advantage: Transmitted bit-depth is decoupled from the video transport clock rate! Where digital transports require frequency to at least double if bit depth is increased from 8 to 16 bits per pixel, SAVT conveys sub-pixels of arbitrary bit depth at unchanged frequency. This leads to improved color resolution and potentially transmitting 12 bits or more per sub-pixel, without using Frame Rate Control time-multiplexing, to generate 68 billion colors or more.

5. Results

HYPHY's 'sampled analog' video transport has been extensively tested, and was first conceptually demonstrated at the March 2022 Display Week I-Zone in San Jose, USA. The technology has proven to be fault-tolerant and robust, making it possible to passively transmit an uncompressed HD video signal over 100 m of Cat6A-UTP cable without significant loss of video fidelity. Based on this success, Hyphy designed and built a DDIC capable of replacing the digital DDICs on existing display panels (figure 4), as well as an FPGA based encoding system for SAVT, and

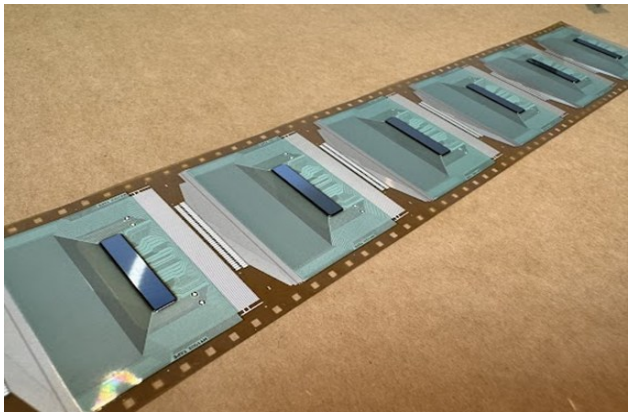

Figure 4: HYPHY HY1002 DDIC

demonstrated its capability to reliably transmit a video signal for an 8K display panel over the normal wiring used for digital drivers in October 2024 (Figure 5).

Figure 5: 65" 8K LCD panel driven by HYPHY HY1002 DDIC

Having repeatedly proven the effectiveness of its innovative approach, HYPHY has embarked on the next stages of its evolution by developing encoding hardware capable of translating a digital video signal into (gamma-corrected) SAVT levels close to its source (i.e. in close proximity to the SOC) as well as further developed driver hardware that is competitive to digital DDICs. Since new digital DDICs need to migrate to faster semiconductor nodes in order to cope with the high data rates (while driver size remains unchanged due to the size of the interconnect), the lower operating frequency and reduced complexity of the HYPHY DDIC will allow manufacturing in the foundries used for generations of DDICs, keeping cost low. It is also envisioned that the transmitter hardware would be available as a design that can be embedded in SOCs for better cost-effectiveness, directly replacing the conventional video transport communication protocols currently used (figure 6).

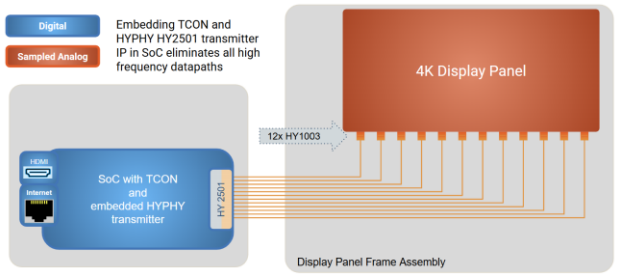

Figure 6: Embedded HYPHY SAVT transmitter

This encoding/driving system will be used in the next generation of high performance UHD displays and mainstream products in the years beyond. Simulations of the DDIC and transmitter hardware currently under development have already demonstrated reduced cost (as described above) and power for SAVT based systems.

6. Impact

HYPHY's unique technological innovation finally removes the 'video throughput barrier' currently stalling the widespread market adoption of high-performance UHD displays. Commercial application of HYPHY's video transmission technology is imminent, and will significantly reduce the manufacturing costs of larger, faster, and more vivid television sets and gaming monitors, and open the route to worry-free high-resolution AR / VR / MR displays by providing a high speed, low EMI video link while maintaining excellent signal robustness, superior video quality, and reduced power consumption.

7. References

[1] Wang, Zhou; Bovik, A.C.; Sheikh, H.R.; Simoncelli, E.P. "Image quality assessment: from error visibility to structural similarity". IEEE Transactions on Image Processing. 13 (4): 600–612 (2004-04-01)

[2] Henzen, Rockoff; Modulated Analog driving of high framerate UHD displays", Proceedings of the SID/DSCC 2023